ALLAMA IOBAL OPEN UNIVERSITY, ISLAMABAD

(Department of Computer Science)

WARNING

- 1. PLAGIARISM OR HIRING OF GHOST WRITER(S) FOR SOLVING THE ASSIGNMENT(S) WILL DEBAR THE STUDENT FROM AWARD OF DEGREE/CERTIFICATE, IF FOUND AT ANY STAGE.
- 2. SUBMITTING ASSIGNMENTS BORROWED OR STOLEN FROM "AIOU PLAGIARISM POLICY".

Course: Digital Logic Design (3409)

Level: Bachelor

Semester: Autumn, 2012

Total Marks: 100

ASSIGNMENT No. 1

Note: All questions are compulsory and carry equal marks.

Q. 1	a	.) (Convert t	he fol	lowing	binary	numb	ers to	decimal	system
------	---	------	-----------	--------	--------	--------	------	--------	---------	--------

i) 10111101

- ii) 1110100
- b) Perform the subtraction with the following decimal numbers using 1's complements and 2's complements.
 - i) 1010100 1000100
- ii) 11101011 1001110

Q. 2 a) Explain the process of following conversions with examples:

- i) Binary to Octal and Hexadecimal
- ii) Octal and Hexadecimal to Binary
- b) Differentiate Map method and Tabulation method in detail. Also discuss difference better Adder and Subtractor.

$$F_1(A,B,C) = A'B + C$$

$$F_2(A,B,C) = AB + A'C + AB'C$$

- b) What are logic gates? Differentiate the following gates AND, OR, NAND and NOR.
- Q. 4 a) Design a combinational circuit that accepts a three-bit number and generates an output binary number equal to the square of the input number.
 - b) Implement the Boolean function:

$$F = AB'CD' + A'BCD' + AB'C'D + A'BC'D$$

With exclusive-OR and AND gates.

- Q. 5 Write a note on each of the following:
 - a) Binary Logic and ICs
 - b) Gates
 - c) Boolean Functions
 - d) Tabulation Method

ASSIGNMENT No. 2

Total Marks: 100

- Q. 1 a) Design a BCD-to-excess-3 code convertor with a BCD-to-decimal decoder and four OR gates.
 - b) Differentiate between full adder and half adder.
- Q. 2 a) Show the logic diagram of a clocked RS flip-flop with four NAND gates.
 - b) Design a counter with the following binary sequence: 0, 1, 3, 7, 6, 4 and repeat. Use T flip-flops.
- Q. 3 a) Differentiate Ripple Counters and Synchronous Counters with the help of an example.
 - b) Differentiate between multiplexer and de-multiplexer.
- Q. 4 a) What is the difference between serial and parallel transfer? What type of register is used in each case?
 - b) Draw the interconnection of I^2L gates to form a 2x4 decoder.
- Q. 5 Write a note on each of the following:
 - a) Memory
 - b) Register Counter
 - c) Decimal Adder
 - d) CMOS

3409 Digital Logic Design

Recommended Book:

Digital Logic Design by Morris Mano

Course Outlines:

Unit-1: Binary System

Binary Numbers Based Conversion of Octal, Hexadecimal and Binary, Complements, Binary Codes, Binary Logic and ICs

Credit Hours: 4 (4+0)

Unit-2: Boolean Algebra and Logic Gates

Definitions, Theorems and Properties, Boolean Functions, Canonical and STD Forms, other Logical Properties, Gates

Unit-3: Simplification of Boolean Function

Map Method, NAND and NOR Implementation, Tabulation Method, Prime Implement

Unit-4: Combination Logic

Design Procedure, Adder, Subtractors, Code Conversation Analysis Procedure, NAND and NOR Functions, Ex-OR and Ex-NOR Function

Unit-5: Combination Logic with MSI and LSI

Binary Parallel Adder, Decimal Adder, BCD Counter, Magnitude Compactor, Decoders, Demultiplexers, Encoder, Multiplexer, ROM, PLA

Unit–6: Sequential Logic

Introduction, Flip Flop, Triggering, State Reduction Excitation Table, Design Procedure, Design of Counter

Unit-7: Register, Counter, and Memory Unit

Register Counter, Timing Sequence, Memory Unit

Unit-8: Asynchronous Sequential Logic

Analysis Procedure, Circuits with Latches, Design Procedure, Reductions of State and Flow Tables, Race Free State Assignment

Unit-9: Digital Integrated Circuits

Bipolar Transistor Characteristics, RTL and DTL Circuits, Transistor, Transistor Logic, Emitter Coupled Logic (ECL), Metal Oxide Semiconductor (MOS), CMOS